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Area Power and Delay Efficient Carry Select Adder (CSLA) Using Bit Excess Technique

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Abstract:

In electronics, an adder or summer is digital circuits that performs addition of numbers and are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. In adder design carry generation is the critical path. To reduce the power consumption of data path we need to reduce Area of the adder. Carry Select Adder is one of the fast adder used in may data path applications. Carry Select Adder (CSLA) is one of the high speed adders used in many computational systems to perform fast arithmetic operations .Due to the rapidly growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). This paper proposes an efficient method. Experimental analysis shows that the proposed architecture achieves the three folded advantages in terms of area, delay and power.

Keywords: CLSA, Adders, VLSI, BEC, Power Consumption, Data.

1.INTRODUCTION :

Adders are most commonly used in various electronic applications e.g. Digital signal processing in which multipliers are used to perform various algorithms like FIR, IIR etc. Earlier, the major challenge for VLSI designer was to reduce area of chip by using efficient optimization techniques to satisfy MOORE'S law. Then the next phase is to increase the speed of operation to achieve fast calculations like, in today's microprocessors millions of instructions are performed per second. Speed of operation is one of the major constraints in designing DSP processors and today's general-purpose processors.

Low-Power, area-efficient, and high-performance VLSI systems are increasingly used in portable and mobile devices, multi standard wireless receivers, and biomedical instrumentation A complex digital signal processing (DSP) system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system. A ripple carry adder (RCA) uses a simple design, but carry propagation delay (CPD) is the main concern in this adder. Carry look-ahead and carry select (CS) methods have been suggested to reduce the CPD of adders.However area and speed are two conflicting constraints. So improving speed results always in larger areas. Now, as most of today's commercial electronic products are portable like Mobile, Laptops etc. that require more battery backup. Therefore, lot of research is going on to reduce power consumption. So, in this paper it is tried to find out the best solution to achieve low power consumption, less area required and high speed for multiplier operation.

Therefore one of the major components required to design Adder is full adder with some logic definition in order to make it a generic one. Adders can be Ripple Carry, Carry Look Ahead, Carry Select, Carry Skip and Carry Save. A lot of research work has been done to analyze performance of different fast adders .In this work, performance analysis of addition by using CLA,RCA,CSLA and modified CSLA logic and SQUARE ROOT CSLA logic is presented. The adders presented in this paper are all modeled by using verilog for 32-bit unsigned data. XILINX ISE v 14.2 is used as synthesis tool and FPGA-SPARTAN VI (XC3S250E) device is selected to get area and power reports. Modelsim XE III 6.2g is used to get timing simulation.

2.CARRY LOOK A HEAD ADDER:

Look ahead carry algorithm speed up the operation to perform addition, because in this algorithm carry for

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the next stages is calculated in advance based on input signals. In CLA, the carry propagation time is reduced to O(log2(Wd)) by using a tree like circuit to compute the carry rapidly. The CLA exploits the fact that the carry generated by a bit-position depends on the three inputs to that position. If 'X' and 'Y' are two inputs then if X=Y= 1, a carry is generated independently of the carry from the previous bit position and if X=Y= 0, no carry is generated. Similarly if X ≠ Y, a carry is generated if and only if the previous bit-position generates a carry. 'C' is initial carry , "S" and "C out" are output sum and carry respectively, then Boolean expression for calculating next carry and addition is:

Pi = Xi xor Yi -- Carry Propagation (1)
Gi = Xi and Yi -- Carry Generation (2)
Ci+1 = Gi or (Pi and Ci) -- Next Carry (3)
Si = Xi xor Yi xor Ci -- Sum Generation (4)

Thus, for 4-bit adder, we can extend the carry, as shown below:

$C_1 = G_0 + P_0 \bullet C_0$ (5)

$C_2 = G_1 + P_1 \bullet C_1 = G_1 + P_1 \bullet G_0 + P_1 \bullet P_0 \bullet C_0$ (6)

$C_3 = G_2 + P_2 \bullet G_1 + P_2 \bullet P_1 \bullet G_0 + P_2 \bullet P_1 \bullet P_0 \bullet C_0$ (7)

$C_4 = G_3 + P_3 \bullet G_2 + P_3 \bullet P_2 \bullet G_1 + P_3 \bullet P_2 \bullet P_1 \bullet G_0 + P_3 \bullet P_2 \bullet P_1 \bullet P_0 \bullet C_0$ (8)

3.CARRY SAVE ADDER:

Basically, carry save adder is used to compute sum of three or more n-bit binary numbers. Carry save adder is same as a full adder. As shown in the Figure.1, here we are computing sum of two 32-bit binary numbers, so we take 32 full adders at first stage. Carry save unit consists of 32 full adders, each of which computes single sum and carry bit based only on the corresponding bits of the two input numbers. Let X and Y are two 32-bit numbers and produces partial sum and carry as S and C as shown in the Table1:

Si = Xi xor Yi (9)
Ci = Xi and Yi (10)

The final addition is then computed as:
1. Shifting the carry sequence C left by one place.
2. Placing a 0 to the front (MSB) of the partial sum sequence S.
3. Finally, a ripple carry adder is used to add these two together and computing the resulting sum.

CARRY SAVE ADDER COMPUTATION

X: 1 0 0 1 1
Y: 1 1 0 0 1
Z: + 0 1 0 1 1
S: 0 0 0 0 1
C: + 1 1 0 1 1
Sum: 1 1 0 1 1 1

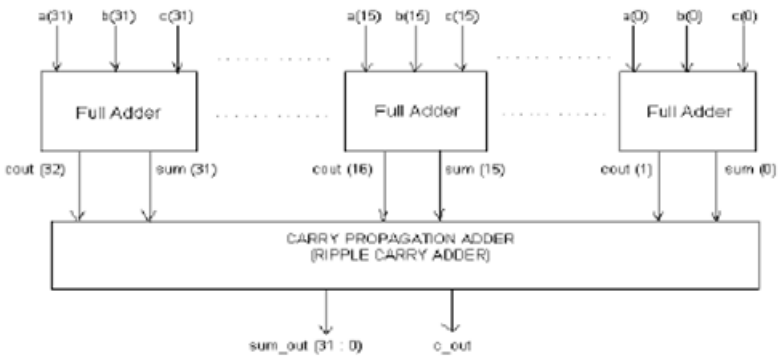

Figure 1. Computation flow of Carry Save Adder

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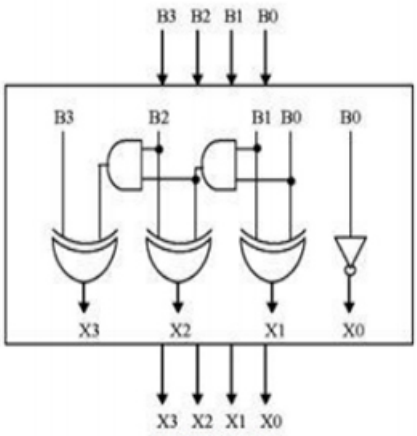
4.BINARY TO EXCESS-1 CONVERTER (BEC):

To reduce the area and power consumption of regular CSLA, RCA with Cin=1 is replaced with BEC. An n+1 bit BEC replaces the n bit RCA. The function table of a 4-b BEC is shown in Fig. 1 and Table 1 respectively. By the use of BEC logic, we can reduce the significant amount of silicon area reduction in the VLSI design. The Boolean expressions of the 3-bit BEC are given below.

S0 = ~ B0
S1 = B0 ^ B1
S2 = B2 ^ (B0 & B1)



4-Bit BEC

5.AREA–DELAY ESTIMATION METHOD:

We have considered all the gates to be made of 2-input AND, 2-input OR, and inverter (AOI). A 2-input XOR is composed 90-nm STANDARD CELL LIBRARY DATASHEET of 2 AND, 1 OR, and 2 NOT gates. The area and delay of the 2-input AND, 2-input OR, and NOT gates (shown in Table I) are taken from the Synopsys Armenia Educational Department (SAED) 90-nm standard cell library datasheet for theoretical estimation. The area and delay of a design are calculated using the following relations:

$$A = a\ Na + r\ No + i\ Ni$$
$$T = na\ Ta + no\ To + ni\ Ti$$

where (Na,No,Ni) and (na, no, ni), respectively, represent the (AND, OR, NOT) gate counts of the total design and its critical path. (a, r, i) and (Ta, To, Ti), respectively, represent the area and delay of one (AND, OR, NOT) gate. We have calculated the (AOI) gate counts of each design for area and delay estimation.

6.Multistage CSLA (SQRT-CSLA):

The multipath carry propagation feature of the CSLA is fully exploited in the SQRT-CSLA , which is composed of a chain of CSLAs. CSLAs of increasing size are used in the SQRT-CSLA to extract the maximum concurrence in the carry propagation path. Using the SQRT-CSLA design, large-size adders are implemented with significantly less delay than a single-stage CSLA of same size. However, carry propagation delay between the CSLA stages of SQRT-CSLA is critical for the overall adder delay. Due to early generation of output-carry with multipath carry propagation feature, the proposed CSLA design is more favorable than the existing CSLA designs for area–delay efficient implementation of SQRT-CSLA.

7.RESULTS :

The simulated waveforms for the different adders is shown in the following figures.

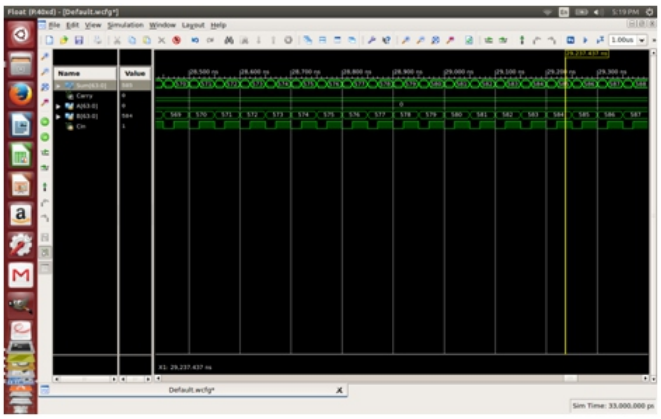


Figure 2. Regular CSLA 64b wave forms

Regular csla consist of ripple carry adders in combination with multiplexer blocks to add up the given two n bit numbers.

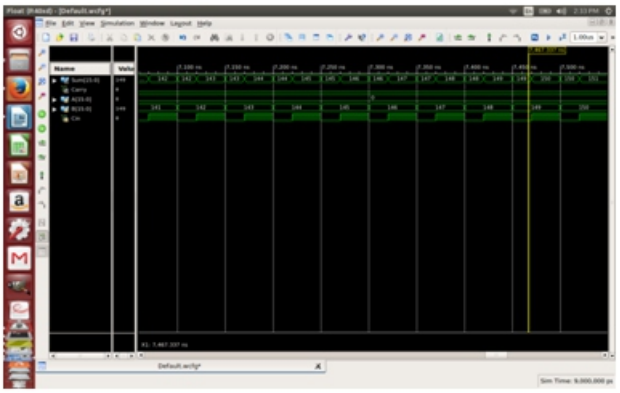


Figure 3. Regual ripple carry adder 32 bits

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This wave form represents the regular ripple carry adder in which we are going to make use of two level full adder cycle to add up two n bit numbers.the number of full adder stages will depends on the number of bits we are making use of to add each other.

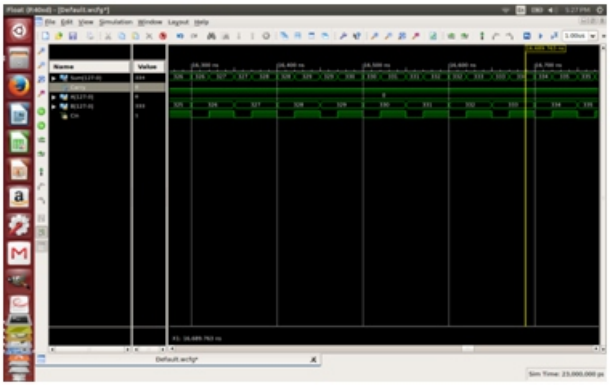

Figure 4. Ripple carry adder 128 bit

This is the regular rca based adder design waveforms in which we are making use of simple full adder chain to add two numbers with 128 bit each.

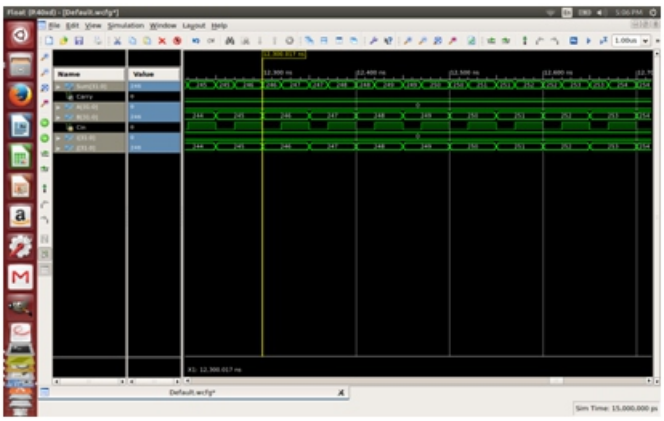

Figure 5. Ripple carry adder 32 bit

This wave form is of the very same ripple carry adder based approach but the bit length varied from 16 bit to 32 bit and we can see the wave forms same as the regular 16 bit rca

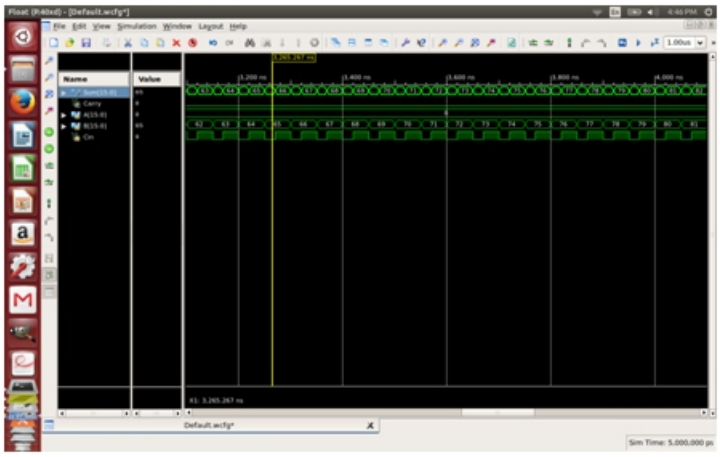

Figure 6 Regular ripple carry adder_16b

This is the regular rca based adder design waveforms in which we are making use of simple full adder chain to add two numbers with 16 bit each.

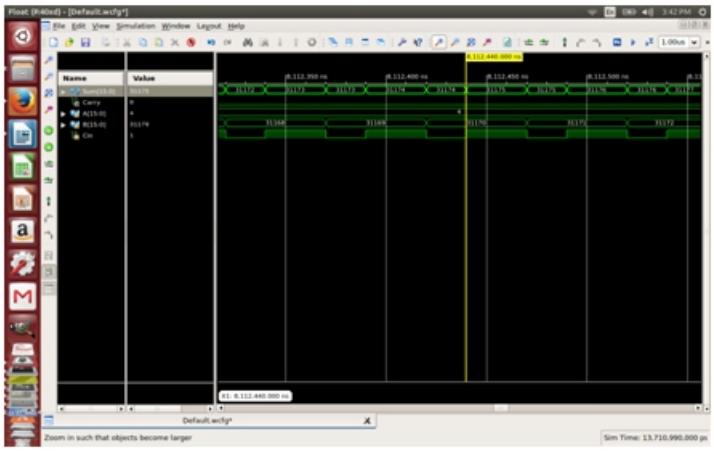

Figure 7 Square root 16 bit BEC based csla

This is the wave form diagram represent the waves of square root csla approach in which we make use of ripple carry adders ,binary to exess-3 converters along with multiplexers in order to add up two n bit numbers.

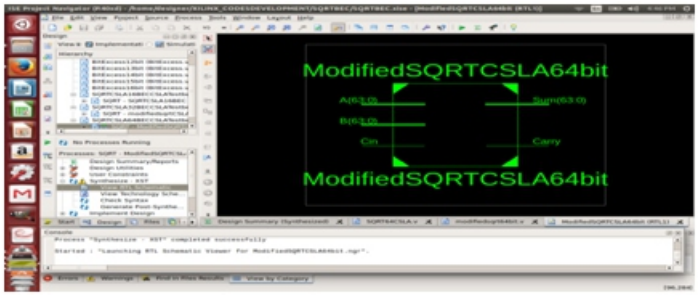

Figure 8 square root csla 64 bit

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This is the RTL schematic view of square root csla structure which consists of the wave forms as shown in above diagram 7.

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